	Ministry of Higher Education and Scientific Research - Iraq Al-Nahrain University College of Science Computer Science Department	

MODULE DESCRIPTOR FORM

نموذج وصف المادة الدراسية

Module Information

معلومات المادة الدراسية

Module Title	DIGITAL LOGIC	**Module Delivery**	
Module Type	CORE		☒**Theory** ☐**Lecture** ☒**Lab** ☐**Tutorial** ☐**Practical** ☐**Seminar**
Module Code	COMP1204		
ECTS Credits	5		
SWL (hr/sem)	125		

Module Level	1	**Semester of Delivery**	2
Administering Department	Computer Science	**College**	Science
Module Leader	Mohammed Sahib Mahdi	**e-mail**	Mohammed.sahibmahdi@nahrainuniv.edu.iq
Module Leader's Acad. Title	Professor	**Module Leader's Qualification**	Ph.D.
Module Tutor	None	**e-mail**	None
Peer Reviewer Name	Prof. Dr. AbdulKareem Merhej	**e-mail**	abdulkareemmerhij@nahrainuniv.edu.iq
Review Committee Approval	15/5/2023	**Version Number**	1.0

Relation With Other Modules

العلاقة مع المواد الدراسية الأخرى

Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	1. The student learns to build logical circuits. 2. The student learns to deal with current, voltage and digital signals 3. The student learns the components and functioning of digital storage units 4. The student learns the work of registration in computers 5. The student learns how to transmit a digital signal between computer components 6. The student learns the components of digital memory and data preservation
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Define the problem (input and output), write its functions. 2. Minimize function using any type of minimizing methods (Boolean algebra, Karnaugh map or Tabulation method). 3. Implement functions using digital circuit (combination or sequential). 4. Have knowledge in analyzing and designing procedures of combinational and sequential circuits. 5. Have knowledge in analyzing and designing circuits with flip-flops, counters and registers. 6. Work effectively with groups.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following: This module introduces the student to understand the digital circuits. [25 hrs] Digital circuits design in computers. [25 hrs] Other topics include: logic circuits, flip flop, registers, RAM. [25 hrs] Some common application circuits of digital RAM types are demonstrated. [25 hrs]

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The length of the semester is 16 weeks, including the exam, and there will be approximately 10٢ hours dedicated to teaching the student the theoretical and practical foundations of the subject of the course, including the theoretical subject, which will take a period of 45 lecture hours (three hours per week) and a practical subject of 30 hours during the course (two hours per week). Two hours are devoted to the mid-term exam, three hours for short exams that extend from the middle to the end of the course, then 20 hours for seminars, homework and the like.

tudent Workload (SWL) الحمل الدراسي للطالب			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	63	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	4.2
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	62	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	4.13
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	125		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	2	10% (10)	5, 10	LO #1
	Assignments	2	10% (10)	2, 12	LO # 2, and 3
	Projects / Lab.	1	10% (10)	Continuous	
	Report	1	10% (10)	13	LO # 4, and 5
Summative assessment	**Midterm Exam**	2 hr	10% (10)	7	LO # 6
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction to Digital Logic Design.
Week 2	Logic Gates and Boolean Algebra: Basic Definition, Boolean Functions.

Week 3	Standard Forms: Minterm and Maxterm, Simplification and Boolean Functions.
Week 4	Logic Operations: NAND,NOR, and Exclusive OR, Integrated Circuits.
Week 5	Gate Level Minimization: The Map Method, Two, Three, and Four variable Map.
Week 6	Product of Sums Simplification, Don't Care Conditions, NAND and NOR Implementation.
Week 7	The Tabulation Method, Simplification of Boolean Functions Using Tabulation Method.
Week 8	Analysis and Synthesis of Combinational Circuits: Combinational Circuits, Analysis and Design Procedure.
Week 9	Binary Adders and Subtractor, Decoders and Multiplexers.
Week 10	Analysis and Synthesis of Sequential Circuits: Sequential Circuits, Latches, Flip-Flops: RS, JK, and D.
Week 11	Analysis of Clocked Sequential Circuits, Design Procedure.
Week 12	Registers and Counters: Registers, Shift Registers, Synchronous Counters, Ripple Counters.
Week 13	Sequential Circuits with programmable Logic Devices: Random Access Memory, Memory Decoding.
Week 14	Read Only Memory, Programmable Logic Array.
Week 15	**Preparatory Week**
Week 16	**Final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Digital Logic Signals.
Week 2	Lab 2: Logic Gates.
Week 3	Lab 3: Logic Operations.
Week 4	Lab 4: Binary Adders and Subtractor.
Week 5	Lab 5: Binary Decoders and Multiplexers.
Week 6	Lab 6: Flip Flop and RS Circuits.
Week 7	Lab 7: Clocked Sequential Circuits.
Week 8	Lab 8: Registers and Counters: Registers.
Week 9	Lab 9: Registers and Counters: Shift Registers, Synchronous Counters.
Week 10	Lab 10: Registers and Counters: Ripple Counters.
Week 11	Lab 11: Random Access Memory,
Week 12	Lab 12: Memory Decoding.

Week 13	Lab 13: Sequential Circuits with programmable Logic Devices
Week 14	Lab 14: Read Only Memory
Week 15	Lab 15: Programmable Logic Array.

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Morris Mano, Charles R. Kime, "Logic and Computer Design Fundamentals", Pearson Prentice Hall,2004.	Yes
Recommended Texts	John F. Wakerly "Digital Design:Principles and Practices Package" 4th edition, Prentice-Hall, 2007.	Yes
Websites	https://sc.nahrainuniv.edu.iq/computers/comp_102.pdf	

APPENDIX:

GRADING SCHEME
مخطط الدرجات

Group	Grade	التقدير	Marks (%)	Definition
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	مقبول بقرار	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note:

NB Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.

ملاحظة: هذا النموذج تم وضعه وتقديمه من قبل مديرية ضمان الجودة في وزارة التعليم العالي والبحث العلمي